Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Applicants gratefully thank Examiner Sefer for the courtesy shown to Applicants' representative during the telephonic interview of May 31, 2007.

Claims 1, 9, 10 and 15 are presently pending in the application. Claim 15 is subject to examination and claims 1, 9 and 10 have been withdrawn from examination. Claim 15 has been amended.

In item 3 of the above-identified Office Action, claim 15 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 5,943,553 to Spaeth et al ("**SPAETH**") in view of Japanese Patent Reference No. JP 2-15897 to Komata et al ("**KOMATA**"). In item 4 of the above-identified Office Action, claim 15 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Japanese Patent Reference No. JP 63-136533 to Kurokawa et al ("**KUROKAWA**") in view of **KOMATA** and U. S. Patent No. 5,234,153 to Bacon et al ("**BACON**").

Applicants respectfully traverse the above rejections, as applied to the amended claim.

More particularly, claim 15 has been amended to recite, among other limitations:

> **a semiconductor chip including, incorporated therein, a doping layer or a contact implantation**, said semiconductor chip having a rear side and an adhesive or diffusion barrier provided on said rear side, **said adhesive or diffusion barrier containing Ti/Pt and being provided directly on said solder**; [emphasis added by Applicant

The above amendment to claim 15 is supported by the specification of the instant application, for example, by Fig. 2B of the instant application, showing the layer sequence, and more particularly, the layer 6 shown therein. The above amendments to claim 15 are additionally supported by the specification of the instant application, for example, on page 9 of the instant application, lines 1 - 11, which state:

> The enlarged partial view shown in Figure 2B shows the sequence of layers in more detail. **A rear side of the semiconductor chip 1 is provided with an adhesion or diffusion barrier 4, which preferably contains Ti/Pt.** Reference numeral 5 denotes a layer of solder that has been sputtered onto the rear side of the wafer with a thickness of typically 1.5 µm. To allow the chip-substrate connection to have a sufficiently low resistance, **it may be necessary for a doping layer, for example of AuAs, or a contact implantation 6 also to have been incorporated beforehand.** [emphasis added by Applicants]

As such, Applicants' claim 15 requires, among other things, a doping layer or contact implantation incorporated into the semiconductor chip and an adhesive or diffusion barrier containing Ti/Pt being provided on the rear side of the

semiconductor, directly on the solder. See, for example, Fig. 2B of the instant application. Additionally, Applicants have amended claim 15 to further recite, among other limitations:

> Sn contained in said solder diffusing away from said solder into adjoining layers, loss of Sn providing a continuous reduction in a melting temperature during a soldering procedure and **resulting in a metallic layer bonded to the semiconductor chip and the substrate, said metallic layer containing Sn**. [emphasis added by Applicants]

As such, Applicants' claim 15 additionally recites the physical limitation of a metallic layer, bonded to the semiconductor chip and the substrate, that contains Sn. This amendment to claim 15 is additionally believed to be supported by the specification of the instant application, for example, on page 8 of the instant application, lines 1 - 7, which state:

> The result is a sufficiently low viscosity of the solder at temperatures of below 380° Celsius for mounting in SOT housings, **since diffusion of Sn into adjoining layers of metal causes the composition of the AuSn to move away from the tin-rich phase toward the eutectic point**, so that a gold-rich solder phase which lies above the eutectic is avoided. [emphasis added by Applicants]

The layers of metal adjoining the AuSn solder, disclosed in the instant application, include the bonding agent or diffusion barrier 4 of Fig. 2B on the semiconductor chip 1 of Fig. 2B, on the one hand, and the substrate 2 of Fig. 2B, on the other hand. As such, Applicants' specification discloses

at least one metallic layer bonded to the semiconductor chip and the substrate, into which the Sn from the solder has diffused, thus resulting in a metal layer containing Sn, as claimed.

None of the prior art references cited in the Office Action teach or suggest the above limitations of Applicants' claim 15, among other limitations. More particularly, in item 3 of the Office Action, Applicants' claim 15 was rejected over the combination of **SPAETH** and **KOMATA**. However, neither **SPAETH**, nor **KOMATA**, teach or suggest, all limitations of Applicants' claim 15. For example, Applicants' amended claim 15 requires, among other limitations, a doping layer or contact implantation incorporated into the semiconductor chip. More particularly, as stated above, page 8 of the instant application, lines 7 - 11 state:

> **To allow the chip-substrate connection to have a sufficiently low resistance**, it may be necessary for a doping layer, for example of AuAs, or a contact implantation 6 also to have been incorporated beforehand. [emphasis added by Applicants]

However, the **SPAETH** and **KOMATA** references fail to teach or suggest such a doping layer or contact implantation incorporated into the semiconductor chip, among other limitations of Applicants' claim.

Further, the **SPAETH** and **KOMATA** references fail to teach or suggest, among other limitations of Applicants' claim, **a semiconductor chip** having an adhesive or diffusion barrier provided on its rear side, **the adhesive or diffusion barrier containing Ti/Pt and being provided directly on said solder**. Rather, the portion of **SPAETH** cited in the Office Action (i.e., col. 3 of **SPAETH**, lines 53 - 60), states:

> For the improvement of the soldering characteristics of the support plate 3 and the semiconductor body 1 and/or the permanence of the solder connective, an electrically conducted bonding agent, **for example TiPt-Au layer sequence**, a TiPd-Au layer sequence or other suitable materials can be deposited on the support plate 3 and/or on the semiconductor body 1. **The Au layer, whose thickness is for example 1 µm, improves the wetting between the solder and Pt or Pd**. [emphasis added by Applicants]

As such, **SPAETH** clearly discloses the use of a TiPT-Au or TiPD-Au **layer sequence**, wherein the Au **layer** "improve the wetting between the solder and Pt or Pd". Thus, **SPAETH** clearly discloses **placing a layer of Au between the solder and the Pt layer**. Thus the teaching in **SPAETH** of placing an Au layer **between** the solder and the Pt containing layer is clearly contrary to Applicants' amended claim 15, which requires, among other limitations, **providing the adhesive or diffusion barrier containing Ti/Pt directly on the solder**.

Further, Applicant has amended Claim 15 to recite, among other limitations, that the diffusion of the solder creates, and

thus that the semiconductor device physically includes, **a metallic layer bonded to the semiconductor chip and the substrate, containing Sn**. The specification of the instant application supports the creation of, and thus, the presence of, this Sn containing metallic layer bonded to the semiconductor chip and the substrate, for example, on page 8 of the instant application, lines 1 - 7. As described therein, the Sn of the solder diffuses into the **bordering** metal layers (i.e., bordering the semiconductor chip and the substrate). Such a Sn containing metallic layer, as presently claimed by Applicants, is neither taught nor suggested in the **SPAETH** reference. Rather, Applicants believe that the TiPT-Au layer sequence of **SPAETH** acts as a diffusion barrier into which the Sn cannot diffuse. Thus **SPAETH** fails to teach or suggest, among other limitations of Applicants' claim 15, **a metallic layer bonded to the semiconductor chip and the substrate, containing Sn**.

The **KOMATA** reference, cited in item 3 of the Office Action in combination with the **SPAETH** reference, does not cure the above-discussed deficiencies of the **SPAETH** reference. For the foregoing reasons, among others, Applicants' claim 15 is believed to be patentable over the **SPAETH** and **KOMATA** references, whether taken alone, or in combination.

Additionally, item 4 of the Office Action rejected Applicants' former claim 15 over the combination of **KUROKOWA**, **KOMATA** and **BACON**. Applicants believe that the amended claim 15 is also patentable over the combination of **KUROKOWA**, **KOMATA** and **BACON**.

More particularly, like the **SPAETH** reference, discussed above, the **KUROKOWA** reference fails to teach or suggest, among other limitations, a doping layer or contact implantation incorporated into the semiconductor chip and an adhesive or diffusion barrier containing Ti/Pt being provided on the rear side of the semiconductor, directly on the solder. For example, the English language abstract of **KUROKOWA**, states:

> ABSTRACT:
>
> PURPOSE: To mount a semiconductor pellet with a gold-tin alloy without varying the characteristics of the circuit element, etc., **by applying and forming an intermediate layer consisting of one selected from at least titanium, chromium and molybdenum onto the semiconductor surface of the pellet.**
>
> CONSTITUTION: A pellet 3 joined by a gold-tin ally layer 4 is brought into contact with said gold-tin alloy layer 4 through an intermediate layer constituted of **a first intermediate layer 9** applied onto the joint surface 3a of the pellet 3 and **composed of titanium** (Ti) and **a second intermediate layer 10 applied to said first intermediate layer 9 and made up of nickel**. To join the semiconductor pallet 3 in which a gold layer 11 is applied onto the second intermediate layer 10 applied onto the first intermediate layer 9 on the joint surface 3a is prepared, and heated at a fixed temperature under the state in which foil 4A consisting of gold-tin alloy is held between said gold layer 11 and the package substrate 1, and the pellet may be scrubbed. [emphasis added by Applicants]

It is clear from the forgoing that, like **SPAETH**, **KUROKAWA** fails to teach or suggest a doping layer or contact implantation incorporated into the semiconductor chip, among other limitations of Applicants' claim 15. More particularly, as stated above, page 8 of the instant application, lines 7 - 11 state:

> **To allow the chip-substrate connection to have a sufficiently low resistance**, it may be necessary for a doping layer, for example of AuAs, or a contact implantation 6 also to have been incorporated beforehand. [emphasis added by Applicants]

No such doping layer or contact implantation, incorporated into the semiconductor chip, is disclosed in the English Abstract of **KUROKOWA**.

Additionally, it is clear from the English language abstract of **KUROKOWA**, that **KUROKOWA** also fails to teach or suggest, among other limitations, using **an adhesive or diffusion barrier containing Ti/Pt being provided on the rear of the semiconductor, directly on the solder**, as required by Applicant's claim 15. Rather, **KUROKOWA** discloses using an intermediate layer consisting of **one** selected from at least **titanium**, **chromium** and **molybdenum** onto the semiconductor surface of the pellet. As such, **KUROKOWA** fails to teach or

suggest, among other limitations of Applicants' claim 15, **an adhesive or diffusion barrier containing Ti/Pt**.

Further, Applicants' claim 15 requires, among other limitations, **the adhesive or diffusion barrier containing Ti/Pt to be provided directly on the solder**. In **KUROKOWA**, the Ti layer 9 is not even provided **directly** on the solder. Rather, as can be seen from Figs. 1a and 1B of **KUROKOWA**, the Ti layer (9 of Fig. 1 of **KUROKOWA**) is separated from the solder (4, 4A of Fig. 1 of **KUROKOWA**) by an adjacent layer of nickel (10 of Fig. 1 of **KUROKOWA**).

Further still, as discussed above, Applicants' amended claim 15 requires, among other limitations, that the diffusion of the solder creates, and thus that the semiconductor device physically includes, **a metallic layer bonded to the semiconductor chip and the substrate, containing Sn**. Rather, as with **SPAETH**, Applicants believe that the nickel layer 10 disclosed in **KUROKOWA** would prevent the diffusion of the Sn from the solder layer 4, 4a into "a metallic layer bonded to the semiconductor chip". Thus, **KUROKOWA** fails to teach or suggest, among other limitations of Applicants' claim 15, **a metallic layer bonded to the semiconductor chip and the substrate, containing Sn**.

The **KOMATA** and **BACON** references, cited in item 4 of the Office Action in combination with the **KUROKOWA** reference, does not cure the above-discussed deficiencies of the **KUROKOWA** reference. For the foregoing reasons, among others, Applicants' claim 15 is believed to be patentable over the **KUROKOWA**, **BACON** and **KOMATA** references, whether taken alone, or in combination.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claim 15. Claim 15 is, therefore, believed to be patentable over the art.

In view of the foregoing, reconsideration and allowance of claim 15 is solicited.

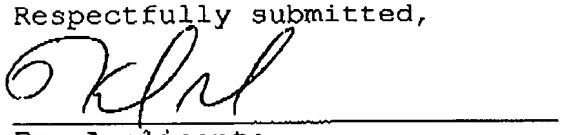
In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Applic. No. 09/483,737
Response Dated November 13, 2007
Responsive to Office Action of August 10, 2007

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



For Applicants

Kerry P. Sisselman
Reg. No. 37,237

November 13, 2007

Lerner Greenberg Stemer LLP
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101